Application No. 09/591,044
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AMENDMENTS TO THE CLAIMS

1. (previously presented) A system for transferring data between a plurality of devices coupled to a bus, at least one of the plurality of devices being operative at a plurality of clock rates, comprising:

a bus including a data line operative to carry data and a clock line operative to carry a clock signal; and

first and second devices operatively coupled to the bus, at least the second device including at least one data register,

wherein the first and second devices are operative at a first clock rate, and the second device is further operative at a second reduced clock rate, the second reduced clock rate being less than the first clock rate,

wherein at least the first device is operative to transmit data over the data line, and

wherein the second device is operative to receive at least a portion of the data transmitted over the data line, to store the at least a portion of the data in the data register, and, in the event the first device is operating at the first clock rate and the second device is operating at the second reduced clock rate, to drive the clock line to a predetermined logic level while the data is stored in the data register, thereby enabling data

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transfer between the first device and the second device over the bus while the second device operates at the second reduced clock rate.

2. (previously presented) The system of claim 1 wherein the second device is further operative at least at the second reduced clock rate to clear the data from the data register upon completion of the data transfer.

3. (previously presented) The system of claim 1 wherein the second device further includes control circuitry for driving the clock line to the predetermined logic level and for releasing the clock line upon completion of the data transfer.

4-5. (canceled)

6. (currently amended) A method of transferring data between a plurality of devices coupled to a bus, at least one of the plurality of devices being operative at a plurality of clock rates, comprising the steps of:

providing ~~first and second devices coupled to~~ a bus and first and second devices coupled to the bus, at least the second device

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including ~~a~~ at least one data register, the first and second devices being operative at a first clock rate, the second device being further operative at a second reduced clock rate, the second reduced clock rate being less than the first clock rate, the bus including a data line for carrying data and a clock line for carrying a clock signal;

~~operating the first device at a first clock rate and operating the second device at a second reduced clock rate, the second reduced clock rate being less than the first clock rate;~~

transmitting data over the data line by the first device;

receiving at least a portion of the data transmitted over the data line by the second device;

storing the at least a portion of the data transmitted over the data line in the data register by the second device; and

in the event the first device is operating at the first clock rate and the second device is operating at the second reduced clock rate, driving the clock line to a predetermined logic level while the data is stored in the data register by the second device, thereby enabling data transfer between the first device and the second device over the bus while the second device operates at the second reduced clock rate.

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7. (currently amended) The method of claim 6 further including the step of clearing the data from the data register upon completion of the data transfer by the second device, the clearing step being performable by the second device operating at least at the second reduced clock rate.

8. (previously presented) The method of claim 6 wherein the driving step includes driving the clock line to the predetermined logic level by control circuitry included in the second device, and further including the step of releasing the clock line upon completion of the data transfer by the control circuitry within the second device.

9. (canceled)

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